REMARKS

Introduction

This Reply is in response to the Office Action of September 30, 2005. Reconsideration of this application in view of the following remarks is respectfully requested.

Claims 1-16, 22-27, and 29

In the Office Action, claim 12 was indicated to contain allowable subject matter. Applicants reserve the right to pursue claim 12 during further prosecution of this patent application should the present remarks not be considered to place the application in condition for allowance.

Claims 1-3 and 7-10 were rejected under 35 U.S.C. § 102(e) as being anticipated by Sia et al. U.S. Patent 6,650,220. Claims 4-5 and 11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sia in view of Ewen U.S. Patent 5,446,311. Claim 6 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Sia in view of Tisharo et al. U.S. Patent 5,515,022. Claims 13, 14, and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sia in view of Chi U.S. Patent 6,362,012. Claim 15 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Sia in view of Chi and Chen U.S. Patent 6,287,931. Claims 22-25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sia in view of

Gillespie et al. U.S. Patent 6,798,039. Claim 26 was rejected as being unpatentable over Sia in view of Gillespie and Li et al. U.S. Patent Publication No. 2002/0177322A1. Claims 27 and former claim 28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sia in view of Patel et al. U.S. Patent 6,429,763. Claim 29 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Sia in view of Patel in view of Chi. These rejections are respectfully traversed.

Claim 1 is directed to an integrated circuit inductor formed in an interconnect dielectric stack on an integrated circuit. The inductor has at least two metal-layer conductive lines that run parallel to each other in respective metal-layer dielectric layers. As set forth in claim 1, the inductor has at least one via-trench conductive line in a via-trench dielectric layer in the interconnect stack. The via-trench conductive line lies between the two metal-layer conductive lines and electrically connects the two metal-layer conductive lines.

Claim 1 therefore explicitly requires that a via-trench conductive line be used to connect the two metal-layer conductive lines. The prior art discloses the use of vias to connect metal-layers, not via-trench conductive lines.

In their specification, applicants explain the advantages of using a via-trench conductive line to connect the two metal lines of the inductor. At page 2, lines 13-22,

applicants describe a conventional inductor arrangement in which an upper-layer line is connected to a lower-layer line by vias. From the surface of an integrated circuit, vias appear as dots, because each via represents a small isolated pillar of metal. The area surrounding each via is filled with an electrical insulator. As explained at page 2, lines 13-22 of applicants' specification, the use of vias to form electrical connections is not sufficiently conductive, so inductors formed using conventional via-based connection arrangements have resistances that are higher than desired. When the resistance of an inductor is too high, the quality factor Q of the inductor is poor.

As set forth on page 4, lines 5-15, with applicants' invention, via trenches form low-resistance electrical paths between the conductive metal-layer lines, because the via trenches run along the length of the conductive metal lines. Vias, in contrast, are one-dimensional dots that are not line-shaped.

Because the use of applicants' via-trench conductive lines lowers the electrical resistance between the inductor's conductive metal-layer lines, inductors fabricated using applicants' via-trench approach are superior to conventional inductors of the via-connection type.

The Sia patent discloses two types of inductors. The first type of inductor is shown in FIGS. 1 and 2. The inductor of FIGS. 1 and 2 in Sia is a conventional inductor using a via-based connection arrangement. As shown in FIGS. 1 and 2 of Sia, connecting vias 24v are used to connect upper layer metal 24 to lower layer metal 24'. Vias 26v (which are mislabeled 22v in FIG. 2), are used to connect upper layer metal 26 to lower layer metal 26'.

The second type of inductor disclosed in Sia is shown in FIGS. 3 and 4. In this type of inductor, the inductor's spirals are connected in parallel to form a parallel stacked inductor 122. Unlike the inductor of FIGS. 1 and 2, the inductor 122 of FIGS. 3 and 4 does not have vias such as vias 22v and 24v that extend between the metal spirals.

In the Office Action, it was suggested that the vias in the inductor of Sia's FIGS. 1 and 2 are the same as the via-trench lines of claim 1. Applicants disagree. The vias in Sia do not have the shape of a line. Vias are small isolated dots, not lines. Because vias are small dots, vias do not present the same surface area as via-trench lines, so vias are not capable of forming the same quality of connection as via-trench lines.

Applicants recognized that conventional via-based connection arrangements of the type described in Sia exhibit relatively high resistivities that pose a problem in forming

high Q inductors. Applicants invented a solution to the high-resistivity via problem by using via-trench lines to connect their metal spirals. The conventional via structures of FIGS. 1 and 2 in Sia are subject to precisely the problem that applicants have solved using their via-trench conductive lines.

Because claim 1 is directed to an inductor in which metal-layer lines are connected using via-trench lines, whereas the metal-layer lines in Sia are connected using vias, claim 1 is patentable over Sia.

Independent claims 22 and 27 are patentable for the same reason as claim 1. The cited references do not make up for the deficiencies of Sia. Claims 2-16 depend from claim 1 and are patentable because claim 1 is patentable. Claims 23-26 are patentable because they depend from claim 22. Claim 29 is patentable because it depends from claim 27.

Claims 30-33

Claim 30 was rejected under 35 U.S.C. § 102(b) as being anticipated by Chen. Claim 31 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Chi. Claims 32 and 33 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Chi and Sia. These rejections are respectfully traversed.

Independent claim 30 relates to using shallow trench isolation to improve inductor performance. As applicants describe at page 18, line 9 to page 19, line 7 of their specification, and as is shown in FIG. 6, a shallow trench isolation (STI) layer 36 may be interposed between the interconnect dielectric stack and the semiconductor substrate. The height H of the interconnect stack 22 is unaffected by the presence of the shallow trench isolation, but a layer of semiconductor of depth D is consumed from the substrate surface at the top of the n-wells 32 and p-wells 34.

The shallow trench isolation is used to help block eddy currents in the semiconductor under the inductor. The use of shallow trench isolation on integrated circuits is well known in other contexts. Shallow trench isolation is a commonly used isolation structure on complementary-metal-oxide-semiconductor (CMOS) integrated circuits. Shallow trench isolation is formed in a silicon substrate by etching a trench of a few tenths of a micron in depth and filling the trench with silicon oxide. The terms "STI" and "shallow trench isolation" are well known in the field of semiconductor processing. Regions of shallow trench isolation are typically used to isolate transistors from each other.

Despite the fact that shallow trench isolation is a commonly understood CMOS structure and is fully compatible with

CMOS processing techniques, shallow trench isolation has not previously been placed under inductors. Applicants, however, have discovered that eddy currents can be reduced by placing this readily-available CMOS structure under the inductor. This obviates the need for forming pits or other structures that are not compatible with standard process flows.

Applicants' use of shallow trench isolation is set forth in claim 30. In particular, claim 30 is directed to an integrated circuit inductor formed of at least two metal lines and shallow trench isolation. According to the language of claim 30, there is a region of shallow trench isolation formed on the surface of a semiconductor substrate under the two metal-layer conductive lines.

In the Office Action, it was suggested that Chen's polymer-filled trench 22 is the same as a region of shallow trench isolation. Applicants disagree.

Chen goes to great lengths to distinguish trench 22 from other structures. For example, trench 22 is referred to by Chen as "deep trench 22." (See, e.g., column 4, lines 10 and 11 of Chen.) Trench 22 is said to be 2-50 microns deep, which is much larger than shallow trench isolation. (See, e.g., column 3, lines 18 and 19 of Chen.) The insulator used to fill trench 22 is also not the same as used for shallow trench isolation. In particular, trench 22 is filled with a carbon-based polymer

such as parylene-F or other insulator having a permitivity less than silicon oxide.

Because claim 30 is directed to an inductor having two metal lines and an region of shallow trench isolation, whereas Chen discloses the use of a deep trench filled with a non-standard insulator, claim 30 is patentable over Chen.

Claims 31-33 depend from claim 30 and are patentable because claim 30 is patentable.

Conclusion

The foregoing demonstrates that claims 1-16, 22-27, and 29-33 are patentable. This application is therefore in condition for allowance. Reconsideration and allowance of the application are respectfully requested.

Respectfully submitted,

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